## REMARKS

Claims 1-4, 14-16, and 20-32 remain pending in this application.

Applicant notes with appreciation the Examiner's indication that claims 1-4 and 21-32 are allowed. With respect to claims 14-16 and 20, review and reconsideration of these claims are respectfully requested.

### Claim Rejections – 35 U.S.C. §103

**The Examiner rejects claims 14-16 and 20 under 35 U.S.C. sec. 103(a) as being unpatentable over U.S. Patent No. 5,689,425 to Sainio et al. in view of U.S. Publication No. 2003/0035547 to Newton. Applicant disagrees.**

With respect to independent claim 14, claim 14 defines a correlator that is implemented substantially in hardware on at least one FPGA. Sainio does not disclose or suggest a correlator that is implemented substantially in hardware. In particular, the correlator described in Sainio is implemented in software, and operates to compare the relative location of a first color mark to that of a second color mark. The correlations described in Sainio are performed in the frequency domain, and the complexity of the Fourier transforms and inverse Fourier transforms dictate that the correlator be implemented in software. Thus, the computer described in Sainio is programmed to perform the correlations. See column 13, lines 3-12 of Sainio.

With respect to Newton, this reference does not describe or suggest an image processing system at all, and does not describe or suggest a correlator. Rather, Newton describes a dedicated hardware encrypter 202 that is implemented on a FPGA.

No motivation exists to combine the Newton reference with the Sainio reference. Without the benefit of hindsight, there is simply no suggestion or motivation for how or why one would desire to implement the software correlator described in Sainio as a FPGA and would look to the hardware encrypter of Newton to do so and thus obtain the invention as defined by Applicant's claim 14. The fact that an encryption system includes a component that has been implemented on a FPGA does not provide sufficient motivation to combine these references.

Therefore, claim 14 is allowable. Claims 15-16 depend from claim 14, and are allowable for at least the reasons discussed above.

With respect to independent claim 20, claim 20 requires, inter alia, an image processing subsystem implemented on at least one FPGA, and wherein when it is desirable to change the image processing subsystem, said at least one FPGA is suitably re-programmed. Neither the Sainio nor Newton references disclose or teach such a re-programmable FPGA in the context of an image processing subsystem. Although Newton does disclose a re-programmable FPGA for performing encryption algorithms, this application does not relate to image processing. As previously stated, no motivation exists to combine the Newton and Sainio references. Accordingly, claim 20 is allowable.

**CONCLUSION**

In view of the foregoing, allowance of claims 14-16 and 20 are respectfully requested. The undersigned is available for telephone consultation at any time.

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